MAR 29 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/798,540	Filing Date:	March 10, 2004
Confirmation No.:	Unassigned		
First Named Inventor:	Sergey Savastiouk		
Assignee:	Tru-Si Technologies, Inc.		
Examiner:	Unassigned	Art Unit:	Unassigned
Attorney Docket No.:	M-15302-1P US		

San Jose, California
March 24, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of documents AA through BB are not enclosed as all documents were previously cited by or submitted to the Patent Office in a prior application relied upon for priority under 35 U.S.C. 120(37 C.F.R. § 1.98(d)). The prior application is U.S. Application No. 10/739,788, filed December 17, 2003. Copies of the remaining documents are enclosed except for the United States Patents and United States Published Patent Applications.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made, other than as described above; or

3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

No fee is believed to be required for this Information Disclosure Statement. If a fee is required, please charge the fee to deposit account 50-2257. This paper is submitted in duplicate.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 24, 2004.

Michael Shenker 3-24-04

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicant(s)
Reg. No. 34,250
Law Offices of MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
(408) 392-9250 x212 (tel)
(408) 392-9262 (fax)
e-mail: mshenker@macpherson-kwok.com

U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Serial No.
	M-15302-1P US	10/798,540
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Savastiouk et al.	
	Filing Date	Group
	March 10, 2004	Unassigned

OIPE MAR 2 9 2004 PATENT & TRADEMARK OFFICE

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	2003/0047798A1	13 Mar 2003	Halahan			
	AB	2003/0226254A1	11 Dec. 2003	Koning et al.			
	AC	2003/0211720A1	13 Nov. 2003	Huang et al.			
	AD	6,498,074	24 Dec. 2002	Siniaguine et al.			
	AE	6,498,381	24 Dec. 2002	Halahan et al.			
	AF	6,322,903	27 Nov. 2001	Siniaguine et al.			
	AG	6,163,456	19 Dec. 2000	Suzuki et al.			

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AH	WO 01/45476 A1	21 Jun. 2001	PCT				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AI	Perfecto, Eric; Lee, Kang-Wook; Hamel, Harvey; Wassick, Thomas; Cline, Christopher; Oonk, Matthew; Feger, Claudius; McHerron, Dale, "Evaluation of Cu Capping Alternatives for Polymide-Cu MCM-D" IEEE, 2001 Electronic Components and Technology Conference.
	AJ	Pang, John H.L.; Chong, D.Y.R.; Low T.H. "Thermal Cycling Analysis of Flip-Chip Solder Joint Reliability" IEEE Transactions on Components and Packaging Technologies, Vol. 24, No. 4, Dec. 2001, pages 705-712.
	AK	Painaik, Mandar; and Hurley, Jim "Process Recommendations for Assembly of Flip Chips Using No-Flow Underfill" Semiconductor Products, Technical Bulletin, www.cooksonsemi.com.
	AL	Ekstrom; Bjorn "Thin Film Silicon Substrates For Lead Frame Packages" Advancing Microelectronics – May/June 2003, pages 6-7.
	AM	Gilleo, Ken "Substrates for Flip Chips" "Flip Chips Technology" in Area Array Packaging Handbook – Manufacturing and Assembly; K Gillio, Editor; The McGraw-Hill Companies, Inc., New York, NY.
	AN	Maiwald, Werner "Soldering SMD's Without Solder Paste" http://www.midwestpcb.com/sales/Kehoe/maiwald.htm.
	AO	"Staychip; 2078E No-Flow Fluxing Underfill; For Solding Sn/Pb eutectic solder bumps to common pad metallizations Preliminary Technical Bulletin" Semiconductor Products, Technical Bulletin; Cookson Electronics.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Serial No.
	M-15302-1P US	10/798,540
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Savastiouk et al.	
	Filing Date	Group
	March 10, 2004	Unassigned

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	AP	"Design Notes: Understanding Ball Grid Array Packages" Electronics by Design, www.electronicsbydesign.com.au, issue 1997.10, pages 1-4.
	AQ	Sperling, Ed; Electronic News, 9/17/2003.
	AR	"Introduction to Printed Wiring Boards" Netpack Education Pool, page 1-18.
	AS	"Production Qualification Report: Select Qual B: Strand Substrate on MCM MQFP Qual" Amkor Technology, Date Released: June 14, 2002.
	AT	"Strand is Closing the Enterprise" Strand Interconnect AB, Viggengatan5, SE-602 09 Norrkoping Sweden, www.strandinter.se.
	AU	"200mm Wafer Fab" Strand Interconnect, Partner for High Performance Electronics.
	AV	Guenin, Bruce M. "The Many Flavors of Ball Grid Array Packages" Electronics Cooling, Feb. 2002, pages 1-7.
	AW	"HPMX-5001: Demonstration Circuit Board: Application Brief 102" Hewlett Packard, pages 1-10.
	AX	Moon, K.W.; Boettinger, W.J.; Kattner, U.R.; Biancaniello, F.S.; Handwerker, C.A. "The Ternary Eutectic of Sn-Ag-Cu Colder Alloys" Metallury Division, Materials Science and Engineering Laboratory NIST Gaithersburg, MD 20899 USA.
	AY	Lu, H. and Bailey, C. "Predicting Optimal Process Conditions for Flip-Chip Assembly Using Copper Column Bumped Dies" School of Computing and Mathematical Sciences, 2002 IEEE, 2002 Electronics Packaging Technology Conference, pages 338-343.
	AZ	Wang, Tie; Tung, Francisca; Foo, Louis; and Dutta, Vivek "Studies on A Novel Flip-Chip Interconnect Structure – Pillar Bump" Advanpack Solutions Pte Ltd, 2001 IEEE, 2001 Electronic Components and Technology Conference.
	BA	United States Patent Application No. 10/739,707, entitled "Packaging Substrates For Integrated Circuits and Soldering Methods," Filed on December 17, 2003; Attorney Docket No.: M-15278 US.
	BB	"Technical Data Sheet: No-Clean Pin-Probe Testable Solder Paste: NC253" www.aimsolder.com.
	BC	Zama, Satoru; Baldwin, Daniel F; Hikami, Toshiya; Murata, Hideaki "Flip Chip Interconnect Systems Using Wire Stud Bumps and Lead Free Solder," 2000 IEEE Electronic Components and Technology Conference, pages 1111-1117.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Serial No.
	M-15302-1P US	10/798,540
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Savastiouk et al.	
	Filing Date	Group
	March 10, 2004	Unassigned

		OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)
	BD	Wang, C.H.; Holmes, A.S.; Gao, S. "Laser-Assisted Bump Transfer for Flip Chip Assembly," 2000 IEEE Int'l Symp on Electronic Materials & Packaging, pages 86-90.
	BE	Gektin, Vadim; Bar-Cohen, Avram; Witzman, Sorin "Coffin-Mason Based Fatigue Analysis of Underfilled DCAs," 1998 IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, Volume 21, No. 4, December 1998, pages 577-584.
	BF	Tran, S.K.; Questad, D.L.; Sammakia, B.G. "Adhesion Issues in Flip-Chip on Organic Modules," 1998 InterSociety Conference on Thermal Phenomena, pages 263-268.
	BG	"Chapter 7: Wedge and Double Cantilever Beam Tests on a High Temperature Melt Processable Polymide Adhesive, TPER-BPDA-PA," pages 221-242.
	BH	"Flip Chip Bonding in Practice" Issue No. 7, September 2001, The Micro Circuit Engineering Newsletter.
	BI	www.flipchips.com/tutorial27.html "Flipchips: Tutorial 27, Shaping Gold Stud Bumps" Pages 1-8.
	BJ	Jordan, Jerry "Gold Stud Bump In Flip-Chip Applications," 2002 Palomar Technologies, Inc.
	BK	Jasper, Jorg "Gold or Solder Chip Bumping, the choice is application dependent" Chip Interconnection, EM Marin, pages 1-4.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.